IETE Warangal sub centre

Welcomes you

For the seminar on

"Basics of Digital VLSI cell design"

- A Tool perspective

By

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In association with

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Aim of the seminar

- To give basics of VLSI design with a general tool usage (schematic editor, layout editor, SPICE etc).
- To give a basic introduction of VLSI design flow.
- To introduce free/open source tools so that every one can work at their home/office.
- This seminar can be considered as introduction to digital VLSI cell level design

VLSI Design

- What is VLSI?
  - "Very Large Scale Integration"
  - Defines integration level
  - 1980s hold-over from outdated taxonomy for integration levels
    - Obviously influenced from frequency bands, i.e. HF, VHF, UHF
  - Sources disagree on what is measured (gates or transistors?)

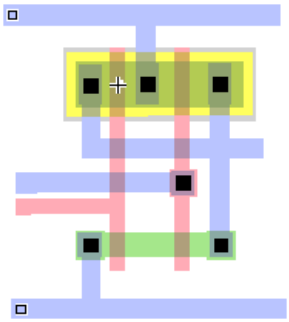
- SSI – Small-Scale Integration (0-10^2)
- MSI – Medium-Scale Integration (10^2 -10^3)
- LSI – Large-Scale Integration (10^3 -10^5)
- VLSI – Very Large-Scale Integration (10^5 - 10^7)
- ULSI – Ultra Large-Scale Integration (>= 10^7)

Chips

- Integrated circuits consist of:
  - A small square or rectangular "die", < 1mm thick
    - Small die: 1.5 mm x 1.5 mm => 2.25 mm^2
    - Large die: 15 mm x 15 mm => 225 mm^2
  - Larger die sizes mean:
    - More logic, memory
    - Less volume
    - Less yield
  - Dies are made from silicon (substrate)
    - Substrate provides mechanical support and electrical common point

VLSI Design

- Draw polygons that represent layers deposited on the substrate
  - More of an art than science



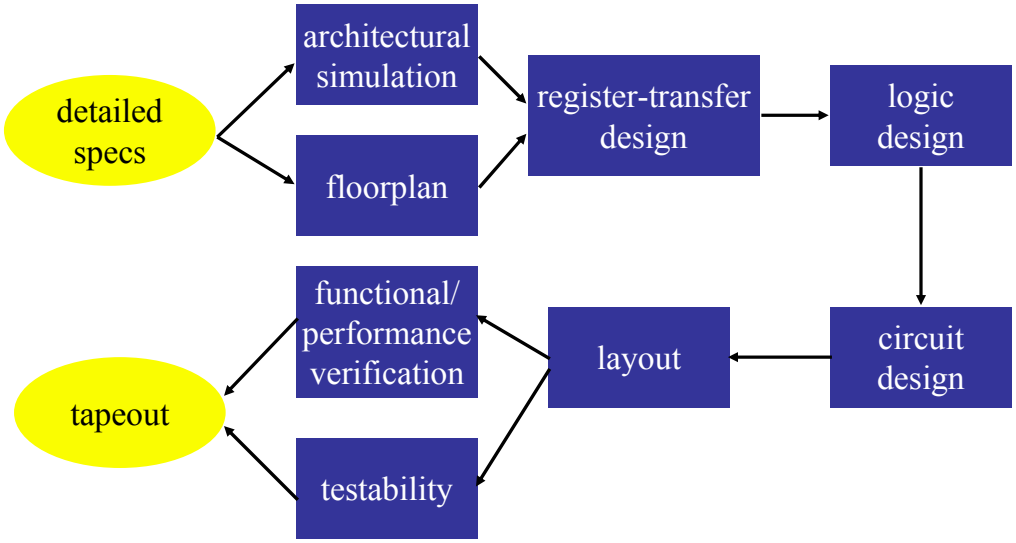
Scale:
approximately
10 um x 10 um

- One 2-input NAND gate with 4 transistors
- Typical microprocessor contains 50 – 200 million transistors (10-50 million gates)

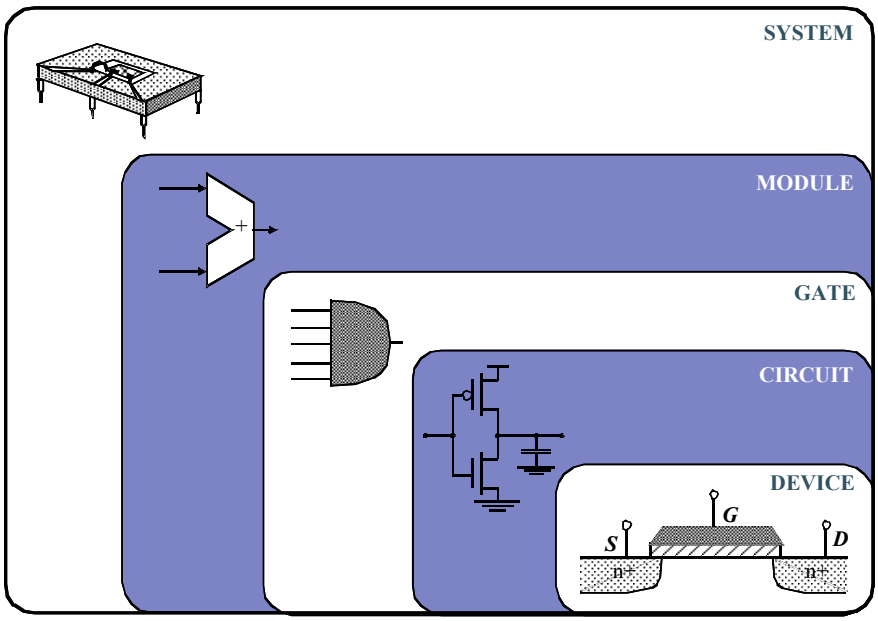
VLSI Design

- Manual layout design is obviously not practical
- Design complexity:
  - Manually drawing layout for a billion transistors would take too long
  - Even if we could…
    - How to verify (test) designs for functionality, speed, power, etc.?
      - Complexity scales faster than actual design
    - How to reuse designs?
    - How to create human-readable designs?
    - How to speed-up design process?
- These problems form a great deal of work
  - Electronic Design Automation (EDA)
- Advancing EDA technology, physical fabrication technology, advanced designs, and IP form bulk of work (and money) in VLSI

Generic design flow



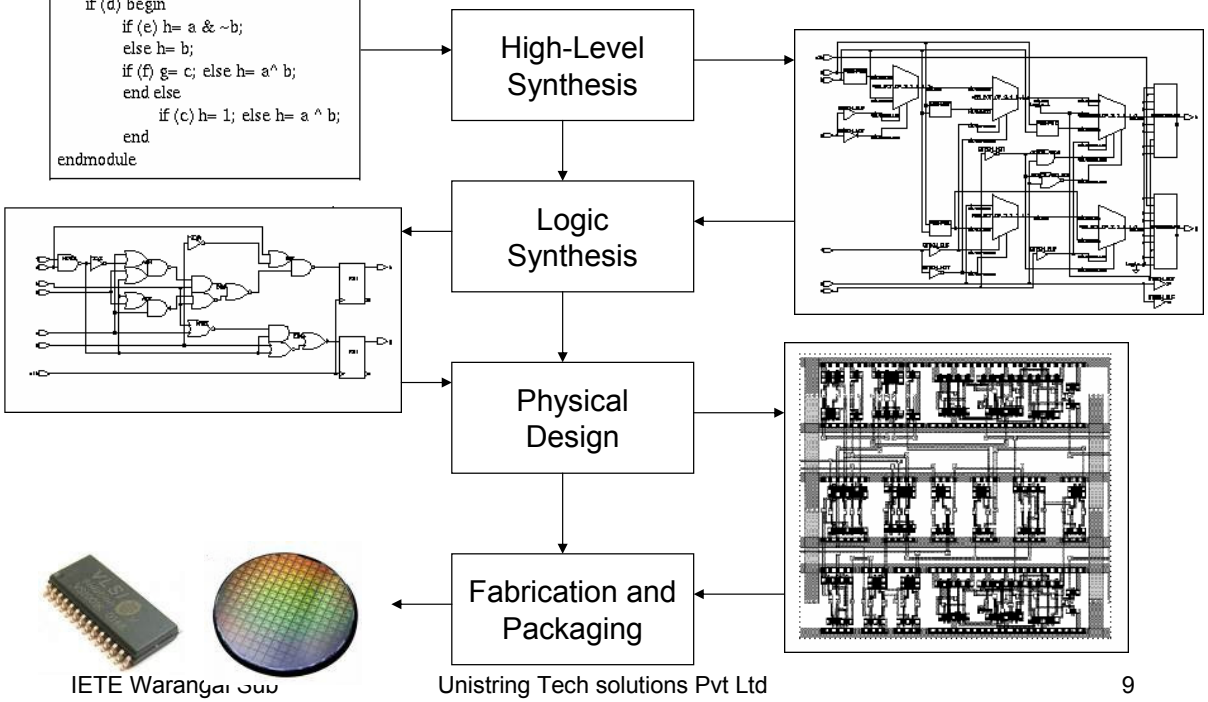
Design Abstraction Levels



Synthesis Flow

```
module example (clk, a, b, c, d, e, f, g, h);
input clk, a, b, c, d, e, f;
output g, h; reg g, h;

always @(posedge clk) begin
    g = a | b;
    if (d) begin
        if (e) h= a & ~b;
        else h= b;
        if (f) g= c; else h= a^ b;
        end else
            if (c) h= 1; else h= a ^ b;
        end
endmodule
```



Electric VLSI design tool

- Open source software
- Schematic and layout editor
- DRC
- LVS
- Can export netlist in various formats
  - SPICE
  - HDL
- Under development

Schematic

- Create a new library
- Set the correct technology (mocmos scale 130nm).
  - File → Preferences → Technology → Scale
- Create a new cell (Ctrl N) “NAND3” - Schematic
- Make a 3 i/p NAND gate
- Create necessary exports (Ctrl E)

Layout

- Create a new cell in the same library - Layout
- Layout name = Schematic name “NAND3”
- From Components choose N-Transistor
- Double click and set L and W
- Rotate (Ctrl J) if necessary
- Array them (F6) to make copies
- Repeat for P- Transistor

Layout

- Decide the orientation of transistors
- Placing vertically may reduce area
- Commonly used components
  - N/P transistor
  - Metal 1 - N/P - Active-contact
  - Metal 1 – N/P – Well contact
  - Metal 1 – Polysilicon – contact
  - Metal N – Metal M – contact
  - **Pure** – N/P Well

Layout - Remember....

- Before you start - check transistor sizes
- Lay the transistors out neatly and carefully
- Look at the schematic and make the connections
- Use minimum metal layers to connect transistors
- Use higher metals for Vdd and Ground
- Make Vdd and Gnd lines thick

Design Rule Check

- Set of spacing/ geometry rules given by the fab
- Have to compulsorily adhere to DRC
- Only then, fab guarantees a working chip
- Check DRC after each step (F5)

Layout Vs Schematic

- Zero DRC does not mean layout is alright
- Easier to verify schematic than layout
- Test schematic thoroughly
- Run LVS test.
  - Tools → NCC → Sch and Lay

After successful DRC and LVS extract SPICE netlist

LT – SPICE
SwCAD - III

Mainly for simulating the circuits with Linear technology chips

Useful for schematic based designs

Cannot be used for layout level design

Works with standard BSIM models

Has a library a general circuit components

Models can be imported into LTSPICE

Please give your valuable feedback …….

Thank you