UTS VLSI forum

VLSI circuit design session - 1
CMOS cell design issues, CMOS logic families.

By

K. Vasu

Senior Application Engineer

VLSI & EH group

Unistring Tech Solutions Pvt. Ltd

 # D10, 5th Floor, Eureka court, Beside Image hospitals, Ameerpet, Hyderabad, ph:040-23732798, 09440318188

www.unistring.com

String Technologies

#309, Vederi complex, opp Dilshuk Nagar bus Depot, Dilsukh nagar, Hyderabad, ph: 040 – 24151900

www.stringtechnologies.net

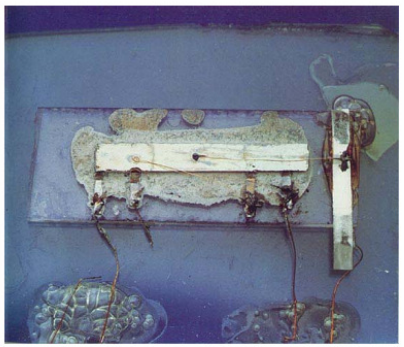
Aim of the seminar

- To give basics of VLSI design with a general tool usage (schematic editor, layout editor, SPICE etc).
- To give a basic introduction of VLSI design flow.
- To introduce free/open source tools so that every one can work at their home/office.
- To give fundamentals of CMOS logic families
- This seminar can be considered as introduction to digital VLSI cell level design

The First IC : 1958

First IC demonstrated by J.S.Kilby of Texas Instruments in 1958

Phase shift oscillator, an analog circuit!



Blue tinge was created by a light shown on the chip.

A thin slice of germanium with

1 bipolar transistor (under the large bar of aluminum in the center),

1 capacitor,

3 resistors (the germanium functioned as its own so-called bulk resistor)

4 input/output terminals (the small vertical aluminum bars)

ground pad (the large bar on the far right), and wires of gold.

Connected together with wax

Actual size: 0.040 x 0.062 inches

CMOS Technology Today (2007)

- 65nm digital technology in volume production
- Number of transistors per chip is ~ 1 billion(DRAMs), ~ 100 million (microprocessors)
- Technology scaling for future is more challenging and expensive
- State of the art fab set-up costs more than US$2 billion
- Recovering the fab cost requires a modular process technology approach capable of producing diverse products

What do we do with the technology capable of making millions of transistor on a tiny area in Si? :

Mixed Signal Systems On Chip (SOC)

VLSI Design

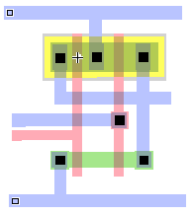
- What is VLSI?
  - "Very Large Scale Integration"
  - Defines integration level
  - 1980s hold-over from outdated taxonomy for integration levels
    - Obviously influenced from frequency bands, i.e. HF, VHF, UHF
  - Sources disagree on what is measured (gates or transistors?)
- SSI – Small-Scale Integration (0-10^2)
- MSI – Medium-Scale Integration (10^2 -10^3)
- LSI – Large-Scale Integration (10^3 -10^5)
- VLSI – Very Large-Scale Integration (10^5 - 10^7)
- ULSI – Ultra Large-Scale Integration (>= 10^7)

Chips

- Integrated circuits consist of:
  - A small square or rectangular "die", < 1mm thick
    - Small die: 1.5 mm x 1.5 mm => 2.25 mm^2
    - Large die: 15 mm x 15 mm => 225 mm^2
  - Larger die sizes mean:
    - More logic, memory
    - Less volume
    - Less yield
  - Dies are made from silicon (substrate)
    - Substrate provides mechanical support and electrical common point

VLSI Design

- Draw polygons that represent layers deposited on the substrate
  - More of an art than science



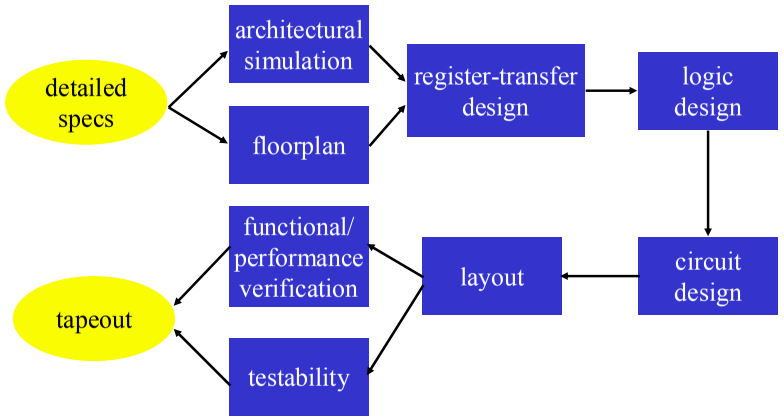
Scale:
approximately
10 um x 10 um

- One 2-input NAND gate with 4 transistors
- Typical microprocessor contains 50 – 200 million transistors (10-50 million gates)

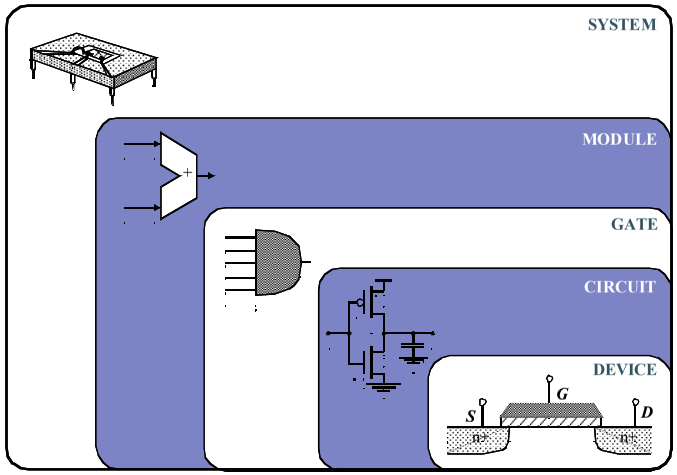
VLSI Design

- Manual layout design is obviously not practical
- Design complexity:
  - Manually drawing layout for a billion transistors would take too long
  - Even if we could…
    - How to verify (test) designs for functionality, speed, power, etc.?
      - Complexity scales faster than actual design
    - How to reuse designs?
    - How to create human-readable designs?
    - How to speed-up design process?
- These problems form a great deal of work
  - Electronic Design Automation (EDA)
- Advancing EDA technology, physical fabrication technology, advanced designs, and IP form bulk of work (and money) in VLSI

Generic design flow



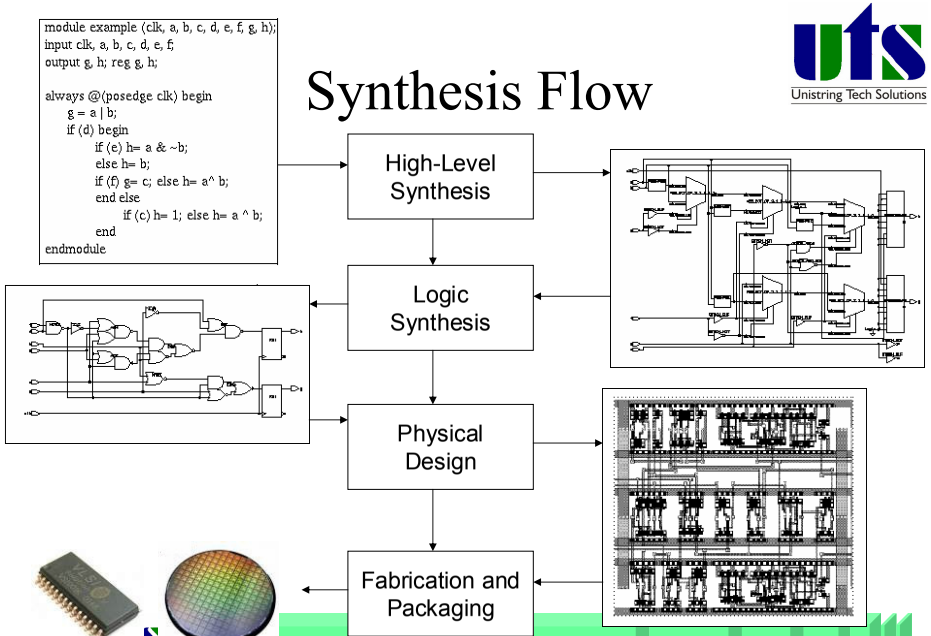
Design Abstraction Levels



Synthesis Flow

```
module example (clk, a, b, c, d, e, f, g, h);
input clk, a, b, c, d, e, f;
output g, h; reg g, h;

always @(posedge clk) begin
    g = a | b;
    if (d) begin
        if (e) h= a & ~b;
        else h= b;
        if (f) g= c; else h= a^ b;
        end else
            if (c) h= 1; else h= a ^ b;
        end
endmodule
```



Electric VLSI design tool

- Open source software
- Schematic and layout editor
- DRC
- LVS
- Can export netlist in various formats
  - SPICE
  - HDL
- Under development

Schematic

- Create a new library
- Set the correct technology (mocmos scale 130nm).
  - File → Preferences → Technology → Scale
- Create a new cell (Ctrl N) "NAND3" - Schematic
- Make a 3 i/p NAND gate
- Create necessary exports (Ctrl E)

Layout

- Create a new cell in the same library - Layout
- Layout name = Schematic name "NAND3"
- From Components choose N-Transistor
- Double click and set L and W
- Rotate (Ctrl J) if necessary
- Array them (F6) to make copies
- Repeat for P- Transistor

Layout

- Decide the orientation of transistors
- Placing vertically may reduce area
- Commonly used components
  - N/P transistor
  - Metal 1 - N/P - Active-contact
  - Metal 1 – N/P – Well contact
  - Metal 1 – Polysilicon – contact
  - Metal N – Metal M – contact
  - **Pure** – N/P Well

Layout - Remember....

- Before you start - check transistor sizes
- Lay the transistors out neatly and carefully
- Look at the schematic and make the connections
- Use minimum metal layers to connect transistors
- Use higher metals for Vdd and Ground
- Make Vdd and Gnd lines thick

Design Rule Check

- Set of spacing/ geometry rules given by the fab
- Have to compulsorily adhere to DRC
- Only then, fab guarantees a working chip
- Check DRC after each step (F5)

Layout Vs Schematic

- Zero DRC does not mean layout is alright
- Easier to verify schematic than layout
- Test schematic thoroughly
- Run LVS test.
  - Tools → NCC → Sch and Lay

After successful DRC and LVS extract SPICE netlist

LT – SPICE SwCAD - III

Mainly for simulating the circuits with Linear technology chips

Useful for schematic based designs

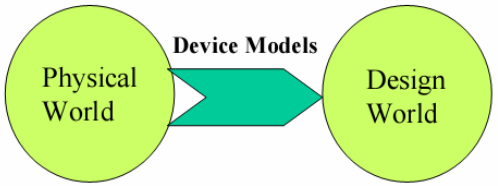
Cannot be used for layout level design

Works with standard BSIM models

Has a library a general circuit components

Models can be imported into LTSPICE

Device Models



- Device models are the links between Technology and Design
- Device models abstract the complete behaviour of the device

Depending on the abstraction accuracy requirement, models with different complexity may be used

Types of Models

Numerical model:

Solve the basic governing equations for the device using numerical techniques (Poisson, Continuity, Transport equations)

Most accurate, but computationally inefficient

Table look up model:

Construct a look up table from the measured results and interpolate the device behaviour

Simple and no equations to be solved, table size grows exponentially with device complexity and the desired accuracy

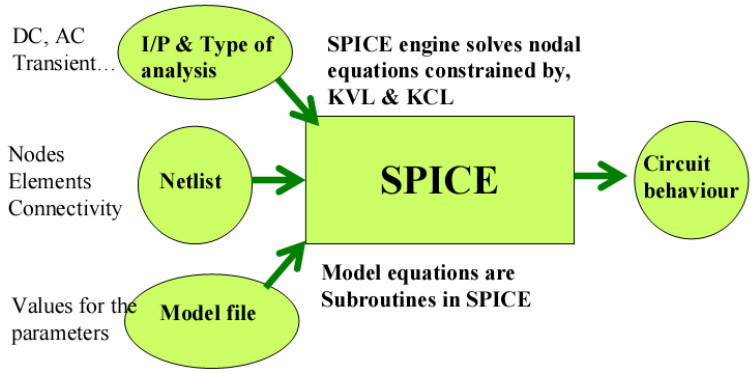
Analytical (Compact) model:

Physics based analytical equations describe the device behaviour

*A set of **model equations** and a set of **model parameters***

"Compact" and used by all the circuit simulators

Simulation Program with Integrated Circuit Emphasis (SPICE)



First SPICE program was released by UC Berkeley in 1973

All the commercial versions are based on this general framework

BSIM3V3.1 for a particular 0.35µm technology

```
.MODEL CMOSN NMOS ( LEVEL   = 49  VERSION = 3.1    TNOM  = 27   TOX  = 7.7E-9
+XJ  = 1E-7       NCH    = 2.2E17   VTH0 = 0.5160489  K1 = 0.5579179     K2  = 0.015461
+K3     = 1E-3 K3B = 0.6729301   W0= 1E-7  NLX = 2.361015E-7 DVT0W= 0     DVT1W = 0
+DVT2W  = 0 DVT0   = 4.6230912     DVT1   = 0.8239238     DVT2   = -0.1545678
+U0 = 420.4056381   UA= -1.37947E-14   UB = 1.541661E-18 UC = 3.740448E-11
+VSAT = 1.726407E5    A0 = 1.1375756  AGS = 0.1469307     B0 = 8.120756E-7   B1= 5E-6
+KETA= 5.121621E-3    A1= 0  A2= 0.4659916 RDSW    = 859.7805695   PRWG   = 3.08832E-4
+PRWB = -0.1474216 WR  = 1   WINT = 8.012725E-8   LINT = 1.415149E-9 XL = -2E-8   XW= 0
+DWG    = -7.030821E-9 DWB    = 9.542202E-9    VOFF   = -0.0957933    NFACTOR = 1.3554507
+CIT = 0  CDSC= 2.4E-4  CDSCD= 0 CDSCB   = 0  ETA0   = 0.3070162     ETAB   = 8.145416E-3
+DSUB = 0.5067323     PCLM = 1.1143333     PDIBLC1 = 1.591971E-3 PDIBLC2 = 7.156257E-3
+PDIBLCB = -1E-3   DROUT   = 0.5162954 PSCBE1  = 7.188166E9    PSCBE2  = 5E-10
+PVAG= 3.892896E-3 DELTA   = 0.01   RSH    = 80.2  MOBMOD  = 1 PRT  = 0  UTE    = -1.5
+KT1    = -0.11 KT1L = 0  KT2= 0.022   UA1= 4.31E-9  UB1 = -7.61E-18     UC1= -5.6E-11
+AT = 3.3E4  WL= 0 WLN= 1  WW = 0 WWN= 1  WWL = 0  LL= 0 LLN = 1  LW = 0  LWN    = 1
+LWL= 0  CAPMOD= 2 XPART   = 0.5 CGDO= 2.84E-10  CGSO= 2.84E-10  CGBO = 1E-12
+CJ = 9.239889E-4   PB = 0.7509356   MJ= 0.3325568 CJSW   = 3.194769E-10  PBSW   = 0.770265
+MJSW   = 0.126513 CJSWG  = 1.82E-10     PBSWG  = 0.770265     MJSWG  = 0.126513
+CF = 0  PVTH0   = -0.0290867    PRDSW  = -167.9120253 +PK2= 3.483917E-3
WKETA   = -6.676585E-5   LKETA   = -5.733128E-3)
```

- **A typical BSIM3V3.2 model has more than 150 model parameters**

Vth Model

$$V_{th} = V_{th0ox} + K_{1ox}\cdot\sqrt{\Phi_s - V_{bseff}} - K_{2ox}V_{bseff}$$
$$+ K_{1ox}\left(\sqrt{1+\frac{Nlx}{L_{eff}}}-1\right)\sqrt{\Phi_s} + \left(K_3 + K_{3b}V_{bseff}\right)\frac{T_{ox}}{W_{eff}'+W_0}\Phi_s$$
$$- D_{VT0w}\left(\exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{2l_{tw}}\right)+2\exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{l_{tw}}\right)\right)\left(V_{bi}-\Phi_s\right)$$
$$- D_{VT0}\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)+2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi}-\Phi_s\right)$$
$$-\left(\exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right)+2\exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)\left(E_{tao}+E_{tab}V_{bseff}\right)V_{ds}$$

Unistring Tech Solutions

Thank you