UTS VLSI forum

Programmable logic devices – Basics & Xilinx FPGA design flow

By

K. Vasu

Senior Application Engineer

VLSI & EH group

Unistring Tech Solutions Pvt. Ltd

 # D10, 5th Floor, Eureka court, Beside Image hospitals, Ameerpet, Hyderabad, ph:040-23732798, 09440318188

www.unistring.com

String Technologies

#309, Vederi complex, opp Dilshuk Nagar bus Depot, Dilsukh nagar, Hyderabad, ph: 040 – 24151900

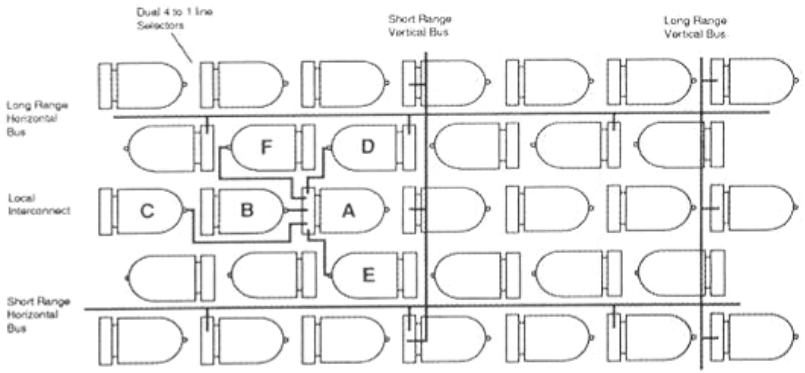
www.stringtechnologies.net

PLDs - Classification by Granularity

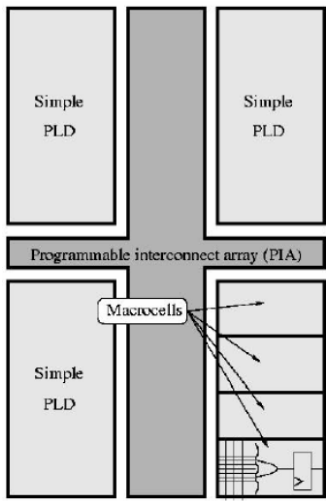
Logic block size correlates to the granularity of a device which, in turn, relates to the effort required to complete the wiring between the blocks (routing channels). In general three different granularity classes can be found

- **Small granularity (sea of gates architecture)**
- **Medium granularity (FPGA)**
- **Large granularity (CPLD)**

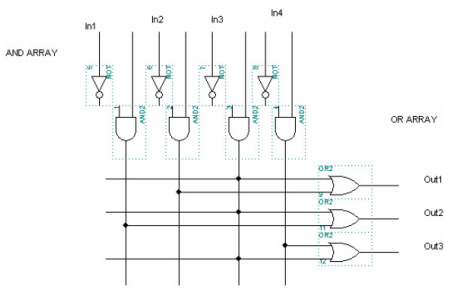
Sea of gates architecture



Complex Programmable Logic Devices (CPLD)



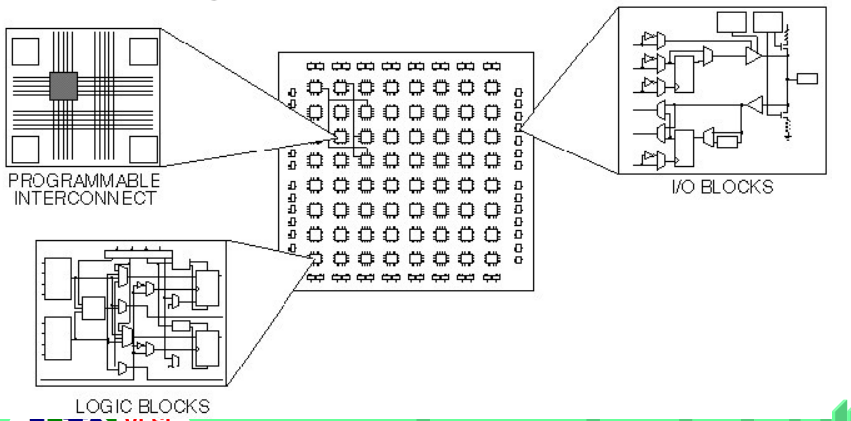
Typically a CPLD consists of 50 SPLDs (An SPLD is a programmable logic array with AND and OR planes)



Programmable Logic Array

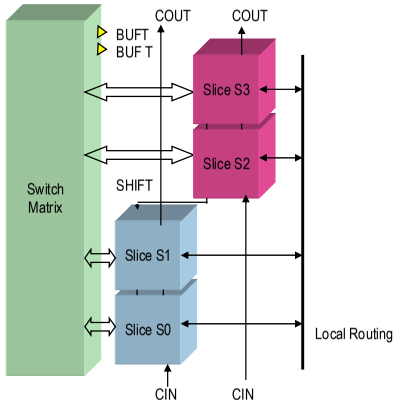
Field Programmable Gate Arrays (FPGA)

Member of class of devices called field programmable logic (FPL). FPLs are defined as programmable devices containing repeated sections of small logic blocks and elements

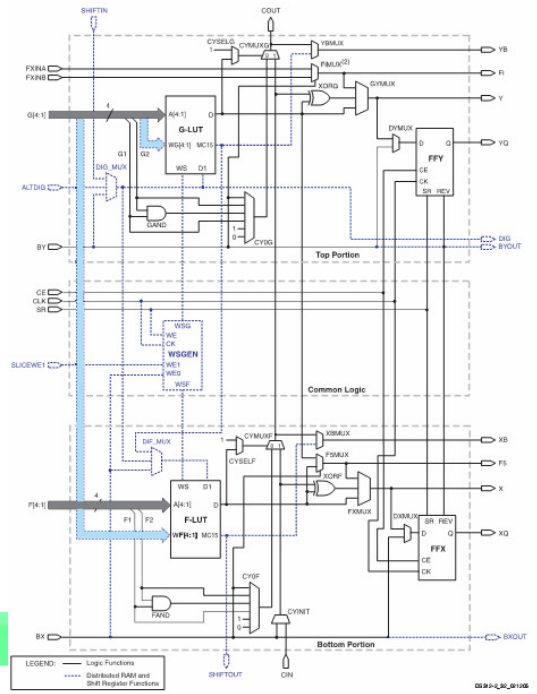


Slices and CLBs

- Each CLB contains four slices
  - Local routing provides feedback between slices in the same CLB, and it provides routing to neighboring CLBs
  - A switch matrix provides access to general routing resources



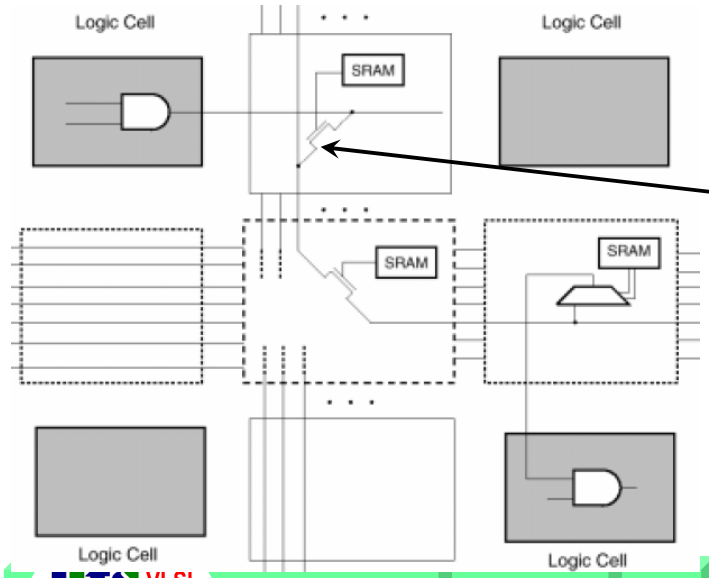
Slice of Xilinx Spartan 3E FPGA



FPGA Programming technologies

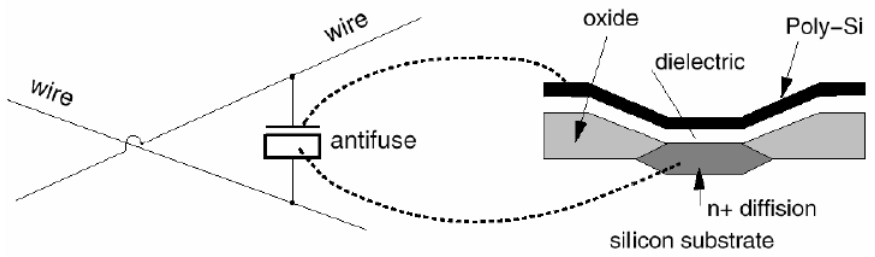
- SRAM.
  - Can be programmed many times.
  - Must be programmed at power-up.
- Antifuse.
  - Programmed once.
- Flash.
  - Similar to SRAM but using flash memory.

SRAM based FPGA



User configurable SRAM based switch

Anti-Fuse based FPGA



Actel Anti-fuse switch technology

FPGA configuration technologies - comparison

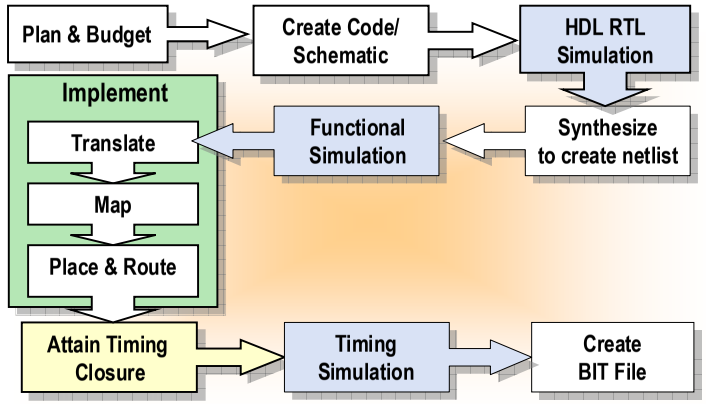
Name	Re-programmable	Volatile	Technology
Fuse	no	no	Bipolar
EPROM	yes out of circuit	no	UVCMOS
EEPROM	yes in circuit	no	EECMOS
SRAM	yes in circuit	yes	CMOS
Antifuse	no	no	CMOS+

Xilinx synthesis and on chip debugging tools

&

A demo on spartan 3E board

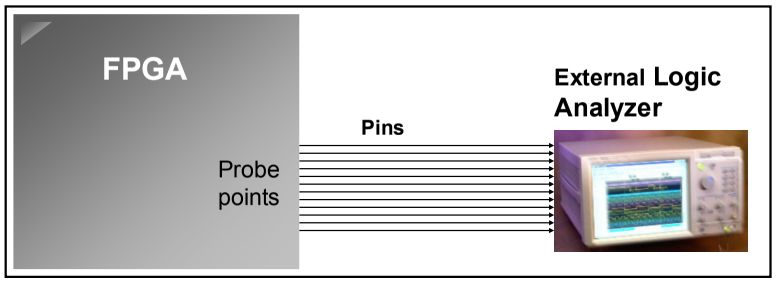
Xilinx Design Flow



Download

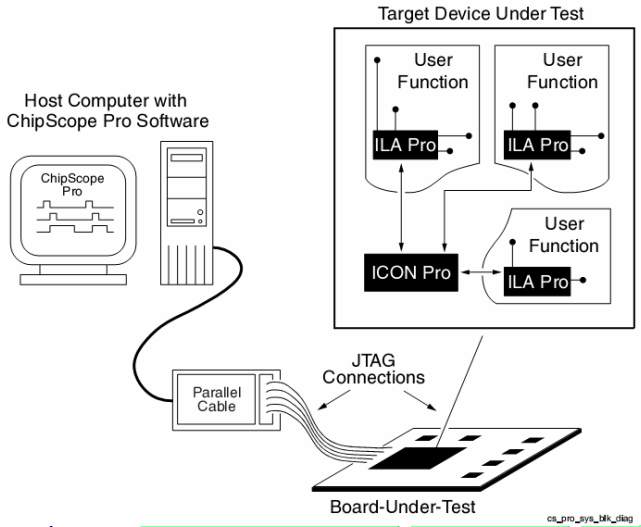
- Once a design is implemented, you must create a file that the FPGA can understand
  - This file is called a bitstream: a BIT file (.bit extension)
- The BIT file can be downloaded directly into the FPGA, or the BIT file can be converted into a PROM file, which stores the programming information

Traditional output verification Or debugging



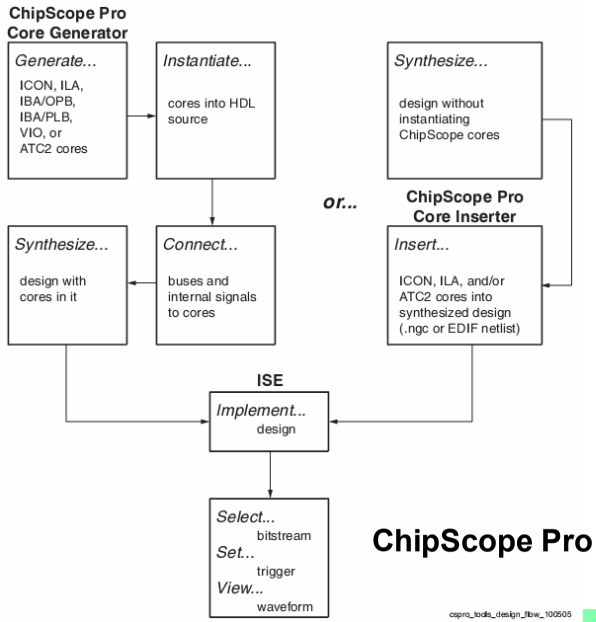
- Requires Extensive Dedicated I/O for Debug
  - Driving signals to external I/O introduces additional problems
- Inflexible solution
  - Difficult or impossible to add additional debug pins if needed
- Limited visibility to on-chip activity

On-Chip Debug with ChipScope Pro



Chipscope Tools

- ChipScope Pro Core Generator
- ChipScope Pro Core Inserter
- ChipScope Pro Analyzer
- Tcl/JTAG Scripting

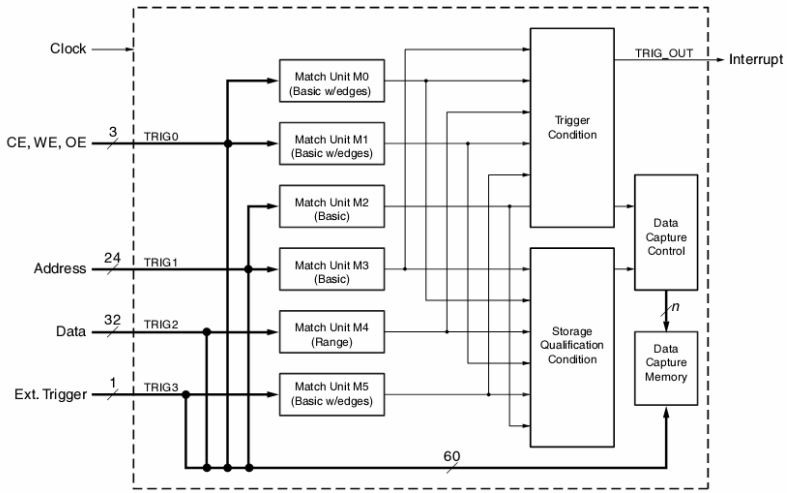


ChipScope Pro Tools Design Flow

ChipScope Pro cores

- Integrated Controller core (ICON)
- Integrated Logic Analyzer core (ILA)
- Integrated Bus Analyzer for CoreConnect On-Chip Peripheral Bus core (IBA/OPB)
- Integrated Bus Analyzer for CoreConnect Processor Local Bus core (IBA/PLB)
- Virtual Input/Output core (VIO)
- Agilent Trace Core 2 (ATC2)

ILA core



Advantages with Chip scope based debugging

- No additional hardware is required
- No I/O pins required for debug
  - Access via the JTAG Port
- On-Chip access to every signal and node in the FPGA design
- Add and remove cores at any time in the design process
- Can be interfaced with Agilent Logic Analyzers

Thank you