UTS VLSI forum

VHDL based design flow

By

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History of VHDL

1981 - Initiated by US DoD to address hardware life-cycle crisis

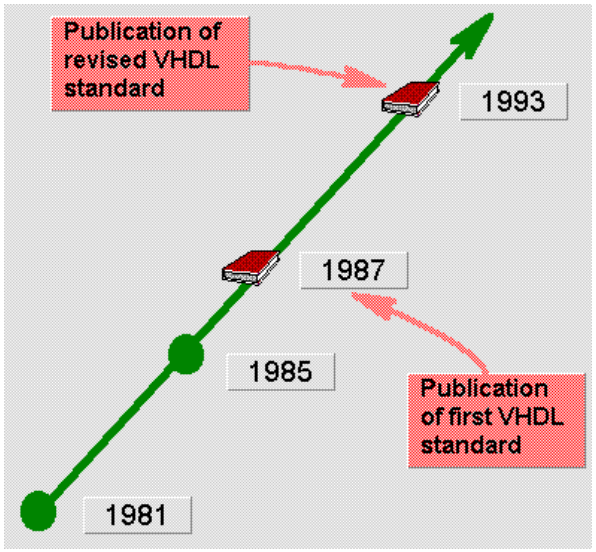
1983-85 - Development of baseline language by Intermetrics, IBM and TI

1986 - All rights transferred to IEEE

1987 - Publication of IEEE Standard

1987 - Mil Std 454 requires comprehensive VHDL descriptions to be delivered with ASICs

1993 - Revised standard (named VHDL 1076-1993)



VHDL

- **VHDL is a Hardware Description Language**
- **VHDL stands for VHSIC Hardware Description Language.**

  (VHSIC stands for Very High Speed Integrated Circuits)
- **Initiated by by United States DOD in the 1980s**
- **The first version was VHDL 87 ; Upgraded to VHDL 93**
- **Standardized by the (IEEE) Institute of Electrical and Electronic Engineers -- IEEE 1076**
- **An additional standard IEEE1164, was later added to introduced multi valued logic system.**
- **VHDL is intended for circuit simulation and as well as circuit synthesis**
- **VHDL is a standard Technology/vendor independent language, and is therefore portable and reusable.**

Design Abstraction Levels

Transistor level - dealing with discrete transistors and connecting them together to form the circuit

Gate level - working with logic gates to build the circuit

register-transfer level - concerned about how the data is transferred between the various registers and functional units to solve the problem at hand

Behavioral level - describing the behavior or operation of the circuit using a hardware description language.

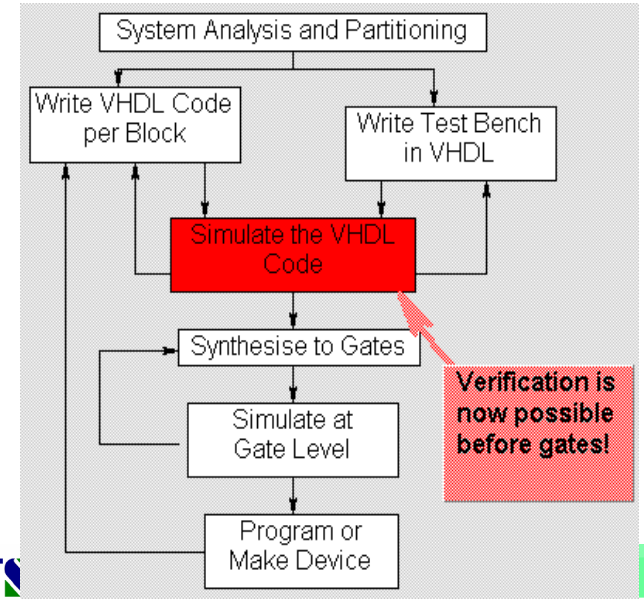
RTL is an acronym for Register Transfer Level

In RTL coding the logic is realized by transferring the data between various registers , with appropriate combinational logic.

This is suitable coding style for several synthesis tools.

70% of design time at RTL in most of the digital designs

Design Flow using VHDL



Simulation

Simulation is a process in which the logic and functional verification of algorithm/design will be verified, by subjecting it to appropriate input test stimulus.

Synthesis

In synthesis the VHDL/Verilog code is translated into low level netlist, to program a device or make a chip.

VLSI Design entry (part of front end design)

In semi custom VLSI design style the required logic can be described by any one, or combination of the following techniques

- Schematic Entry
- Hardware Description Languages
  - VHDL
  - Verilog
  - AHDL
- State machine models
- High level programming languages (latest trend)
  - systemC (C++ class library with Verilog syntax)
- Few Other techniques

VLSI Synthesis (or) Back end Design

In semi custom VLSI design style the required logic (which is in suitable form) can be synthesized for any one of the following devices.

- FPGAs
- CPLDs

} PLD synthesis

- using ASIC cell libraries

} ASIC synthesis

- Gate Arrays

} Structured ASIC synthesis

VHDL code structure

A simple VHDL code consists of at least three fundamental sections

Library declarations

contains a list of all libraries and packages to be used in the design

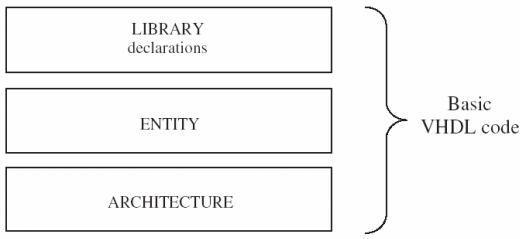
For eg ieee, work, std etc

Entity

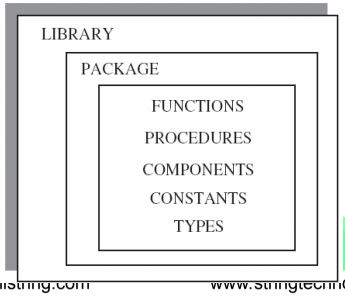
Entity specifies the I/O ports of the circuit

Architecture

Contains the VHDL code, which describes how the circuit should behave




```
LIBRARY library_name;
USE library_name.package_name.package_parts;
```



```
LIBRARY ieee;                    -- A semi-colon (;) indicates
USE ieee.std_logic_1164.all;     -- the end of a statement or

LIBRARY std;                     -- declaration, while a double
USE std.standard.all;            -- dash (--) indicates a comment.

LIBRARY work;
USE work.all;
```

The libraries *std* and *work* shown above are made visible by default, so there is no need to declare them; only the *ieee* library must be explicitly written. However, the latter is only necessary when the STD_LOGIC (or STD_ULOGIC) data type is employed in the design

Three styles of modeling

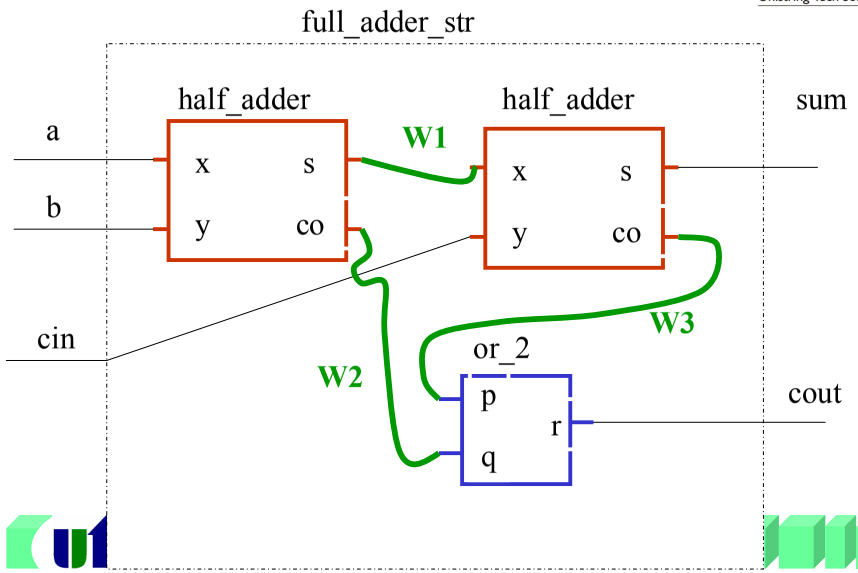
- Data flow style of modeling
- Structural style of modeling
- Behavioral style of modeling


```
-- This is dataflow style of full adder VHDL code
entity full_adder_dat is
       port(a,b,cin:in bit;
            sum,cout:out bit);
end full_adder_dat;

architecture arc_full_adder_dat of full_adder_dat is
begin
      sum <= a xor b xor cin;
      cout<= (a and b) or (b and cin) or (a and cin);
end arc_full_adder_dat;
```

concurrent statements

Structure modeling style of Full Adder



```
-- This is structural implementaion of full adder
entity full_adder_str is
      port(a,b,cin:in bit;
           sum,cout:out bit);
end full_adder_str;
architecture arc_full_adder_str of full_adder_str is
      component half_adder is
           port(x,y:in bit;
                s,co:out bit);
      end component;
      component or_2 is
           port(p,q:in bit;
                r:out bit);
      end component;
      signal w1,w2,w3:bit;
begin
      HA1: half_adder port map(a,b,w1,w2);
      HA2: half_adder port map(w1,cin,sum,w3);
      gate1: or_2 port map(w3,w2,cout);
end arc_full_adder_str;
```



```
-- This is half adder component which is used in
--                              full_adder_str.vhd

entity half_adder is
      port(x,y: in bit;
           s,co:out bit);
end half_adder;

architecture arc_half_adder of half_adder is
begin
      s <= x xor y;
      co <= x and y;
end arc_half_adder;
```



```
-- This is OR gate component which is used in
--                              full_adder_str.vhd
entity or_2 is
      port(p,q:in bit;
           r:out bit);
end or_2;

architecture arc_or_2 of or_2 is
begin
      r<= p or q;
end arc_or_2;
```



```
-- This is behavioural style code for full adder

entity full_adder_beh is
      port(a,b,cin:in bit;
           sum,cout:out bit);
end full_adder_beh;

architecture arc_full_adder_beh of full_adder_beh is
begin
      process(a,b,cin)
      begin
           sum<= a xor b xor cin;
           cout<= (a and b) or (b and cin) or (a and cin);
      end process;
end arc_full_adder_beh;
```

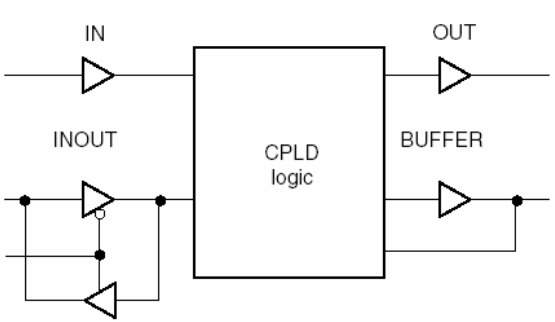
Sequentially executed statements

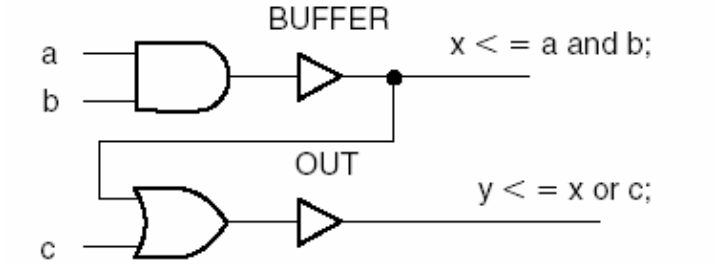
Sensitivity list

Process Statement

- The process statement consists of a number of parts.
- The first part is called the sensitivity list; the second part is called the process declarative part; and the third is the statement part.
- In the preceding example, the list of signals in parentheses after the keyword **PROCESS** is called the sensitivity list.
- This list enumerates exactly which signals cause the process statement to be executed.

Port Modes in VHDL





- The above figure shows the difference between BUFFER and OUT modes.
- Port x (defined by x <= a and b;) must be of mode BUFFER because it is fed back and used as part of the expression for port y (defined by y <= x or c;).
- Port y can be of mode OUT since it has no feedback, only an output.

Thank you