UTS VLSI forum

VLSI Design methodologies

By

K. Vasu

Senior Application engineer

vasu@unistring.com, vasu.vlsi@gmail.com

Unistring Tech Solutions Pvt. Ltd

 # D10, 5th Floor, Eureka court, Beside Image hospitals, Ameerpet, Hyderabad, ph:040-23732798, 09440318188

www.unistring.com

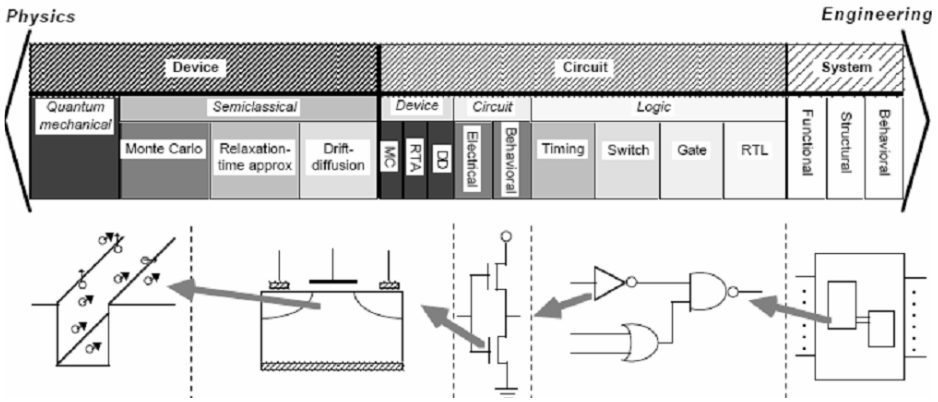
String Technologies

#309, Vederi complex, opp Dilshuk Nagar bus Depot, Dilsukh nagar, Hyderabad, ph: 040 – 24151900

www.stringtechnologies.net

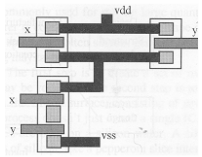
The Big picture

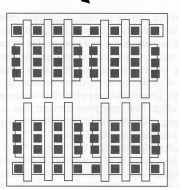
Electron → System

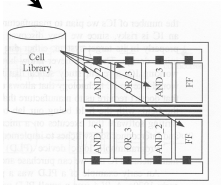


VLSI design Methodologies

- Full-Custom VLSI Design
- Semi-Custom VLSI Design
  - Standard cell based IC technology
  - Structured ASIC IC technology
  - Programmable Logic Device (PLD) IC technology







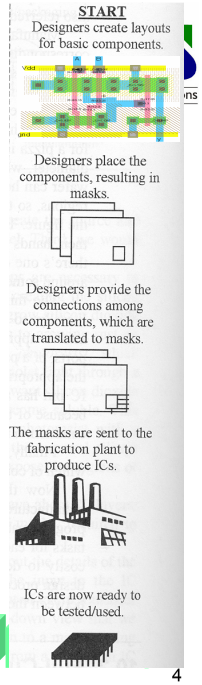
Full Custom design

Designer hand draws geometries which specify transistors and other devices for an integrated circuit.

Designer must be an expert in VLSI (Very Large Scale Integration) design.

Can achieve very high transistor density (transistors per square micron); unfortunately, design time can be very long (multiple months).

Involves the creation of a completely new chip, which consists of about a dozen masks (for the photolitographic manufacturing process).

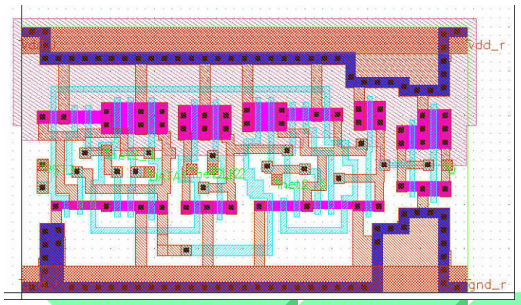


Issues in Full Custom design (continued ..)

- Offers the chance for **optimum performance**.
  - Performance is based on available process technology, designer skill, and CAD tool assistance.
- Fabrication costs are high - all custom masks must be made so non-recurring engineering costs (NRE) is high (in the thousands of dollars).
  - If required number of chips is high then can spread these NRE costs across the chips.
- The first custom chip costs you about $200,000, but each additional one is much cheaper.

Issues in Full Custom design (continued ..)

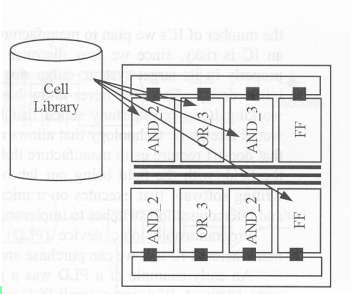
- Fabrication time from geometry submission to returned chips is at least 6-8 weeks.
- Full custom is currently the only option for mixed Analog/Digital chips.
- An example VLSI layout is shown below.



Semi-Custom standard cell based IC Technology

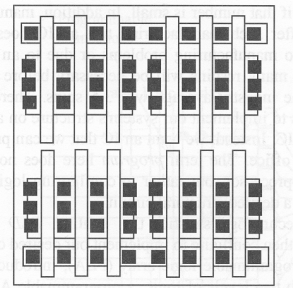
- Standard Cell
  - A library of pre-designed cell
  - Place and route
  - Integrate to yield final layout

ASIC



Semi-Custom Gate Arrays Technology

- Gate Arrays
  - –Array of prefabricated gates
  - –"place" and route
  - –Higher density, faster time-to-market
  - –Does not integrate as well with full-custom

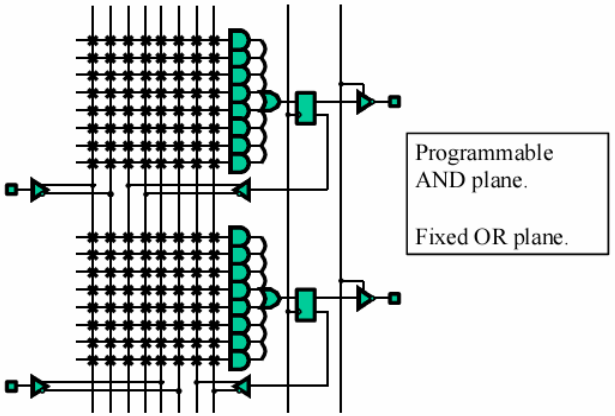


Structured ASIC

Semi-custom Programmable Logic Device (PLD) IC Technology

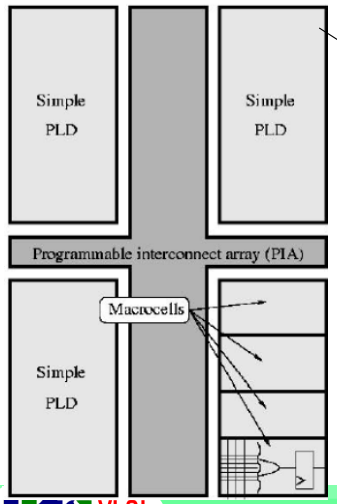
- PAL
- CPLD
- FPGA

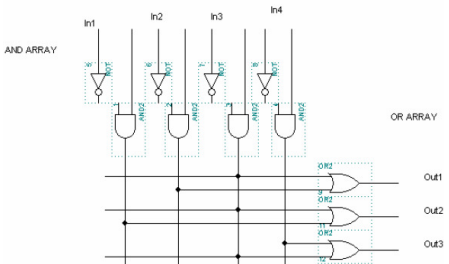
PAL Architecture



Complex programmable logic device (CPLD)

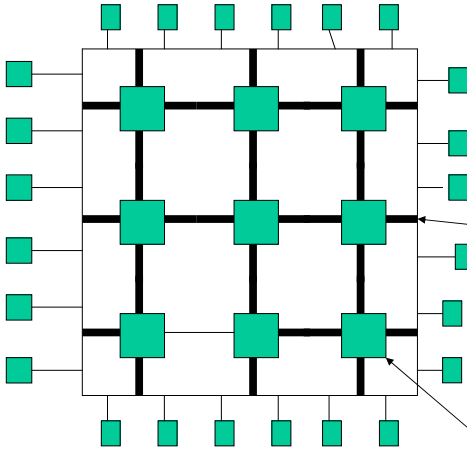
Typically a CPLD consists of few tens to few hundreds of PALs





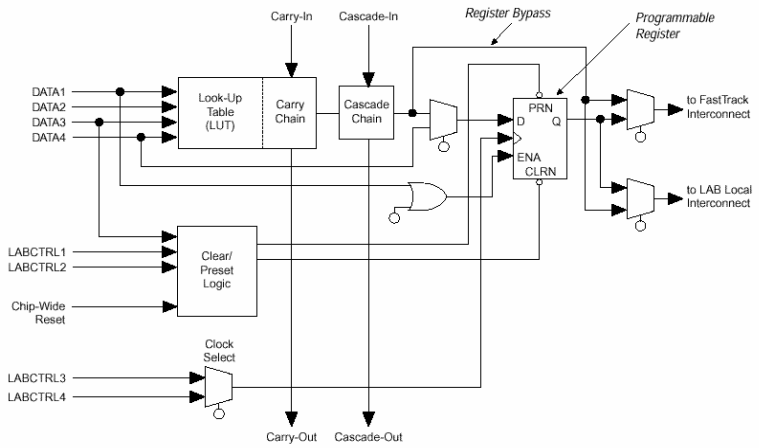
Programmable Logic Array

Field programmable gate array (FPGA)

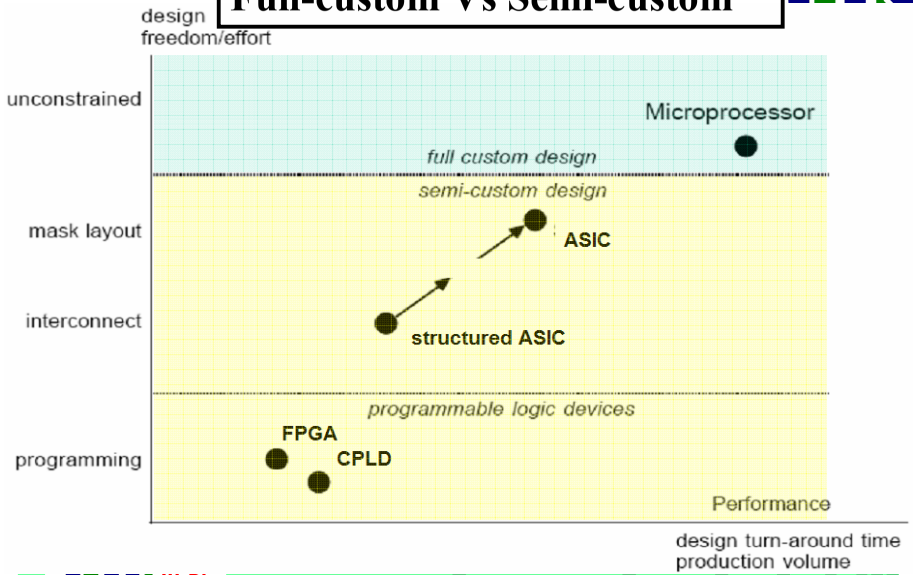


Altera FLEX 10K logic cell

Figure 6. FLEX 10K Logic Element



Full-custom Vs Semi-custom



Semi custom VLSI Design entry (part of front end design)

In semi custom VLSI design style the required logic can be described by any one, or combination of the following techniques

- Schematic Entry
- Hardware Description Languages
  - VHDL
  - Verilog
  - AHDL
- State machine models
- High level programming languages (latest trend)
  - systemC (C++ class library with Verilog syntax)
- Few Other techniques

Semi custom VLSI Synthesis (or) (part of Back end Design)

In semi custom VLSI design style the required logic (which is in suitable form) can be synthesized for any one of the following devices.

- FPGAs
- CPLDs

} PLD synthesis

- using ASIC cell libraries

} ASIC synthesis

- Gate Arrays

} Structured ASIC synthesis

RTL simulation (front end) Tools

Modelsim	Mentor Graphics
VCS	Synopsys
NCSim	Cadence
Max+Plus II simulator	Altera
Xilinx Simulator	Xilinx

synthesis (back end) tools

DC (design compiler)	Synopsys	(ASIC)
PKS (physically knowledgable synthesis)	Cadence	(ASIC)
Synplify Pro	Synplicity	(FPGA)
Xilinx Synthesis technology (XST)	Xilinx	(FPGA)
Altera synthesis tool	Altera	(FPGA)
LeonardoSpectrum	Mentor Graphics (CPLD, FPGA, or ASIC)	

Thank you